Building Executable Specifications using Model Based Design

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AGENDA

- OLD WORKFLOW
- PROBLEM STATEMENT
- NEW WORKFLOW
- RESULTS ACHIEVED

OLD WORKFLOW

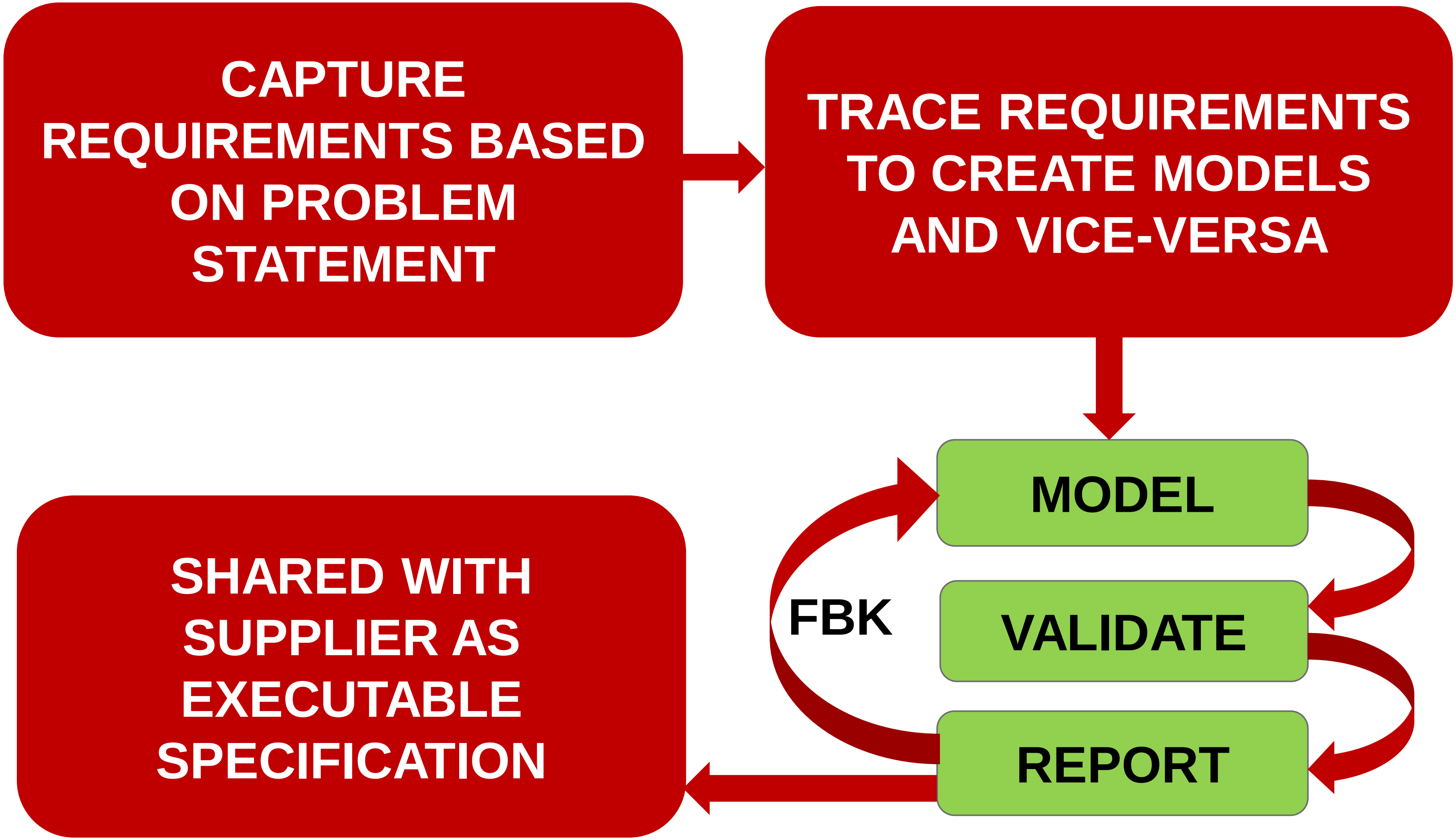
DO A COMPLETE ANALYSIS OF WHAT IS REQUIRED AND DOCUMENT THEM MANUALLY

GIVE THIS AS A REQUIREMENT TO THE SUPPLIER DIRECTLY

PROBLEM STATEMENT

- **Communication gap as most of our suppliers are from North-East Asia**
- **Huge development time**
- **Delay in software deliveries**
- **Numerous software bugs**

NEW WORKFLOW



CAPTURE REQUIREMENTS

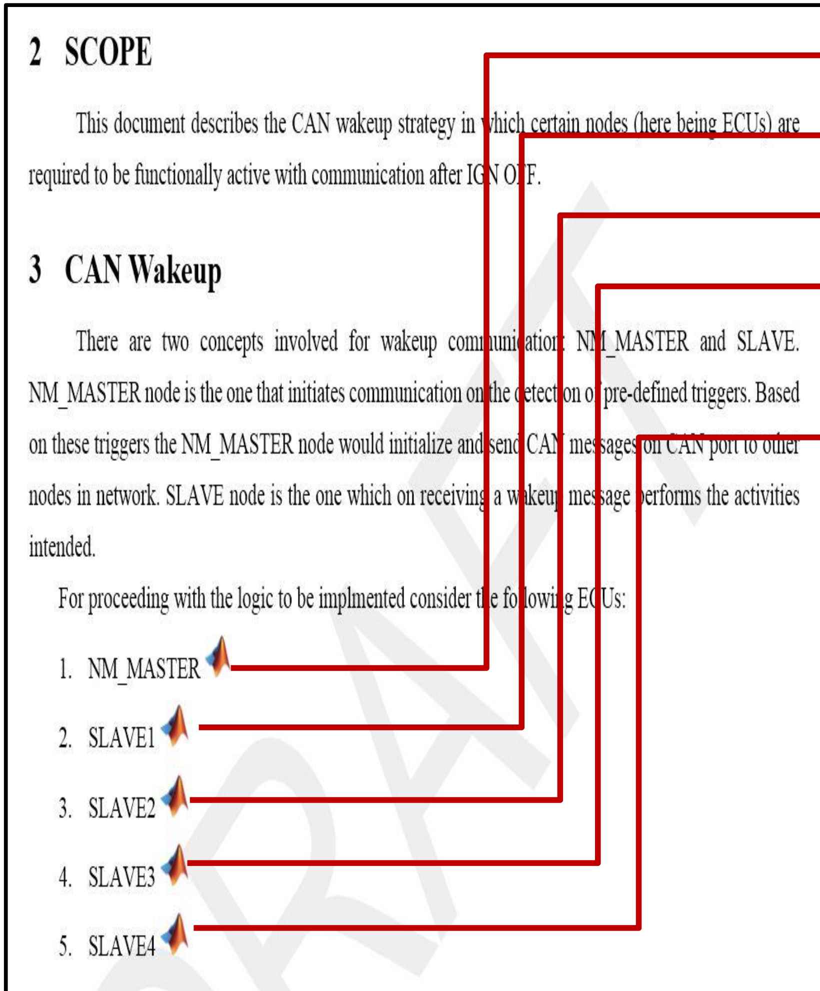
- Communication gap as most of our suppliers are from North-East Asia

→ VAST TEXTUAL CONTENT, NEED FOR MAKING IT MORE ILLUSTRATIVE

- Huge development time
- Delay in software deliveries
- Numerous software bugs

MAKE THE SPECIFICATION VISIBLE AND EXECUTABLE

REQUIREMENT TRACEABILITY AND MODELLING



2 SCOPE

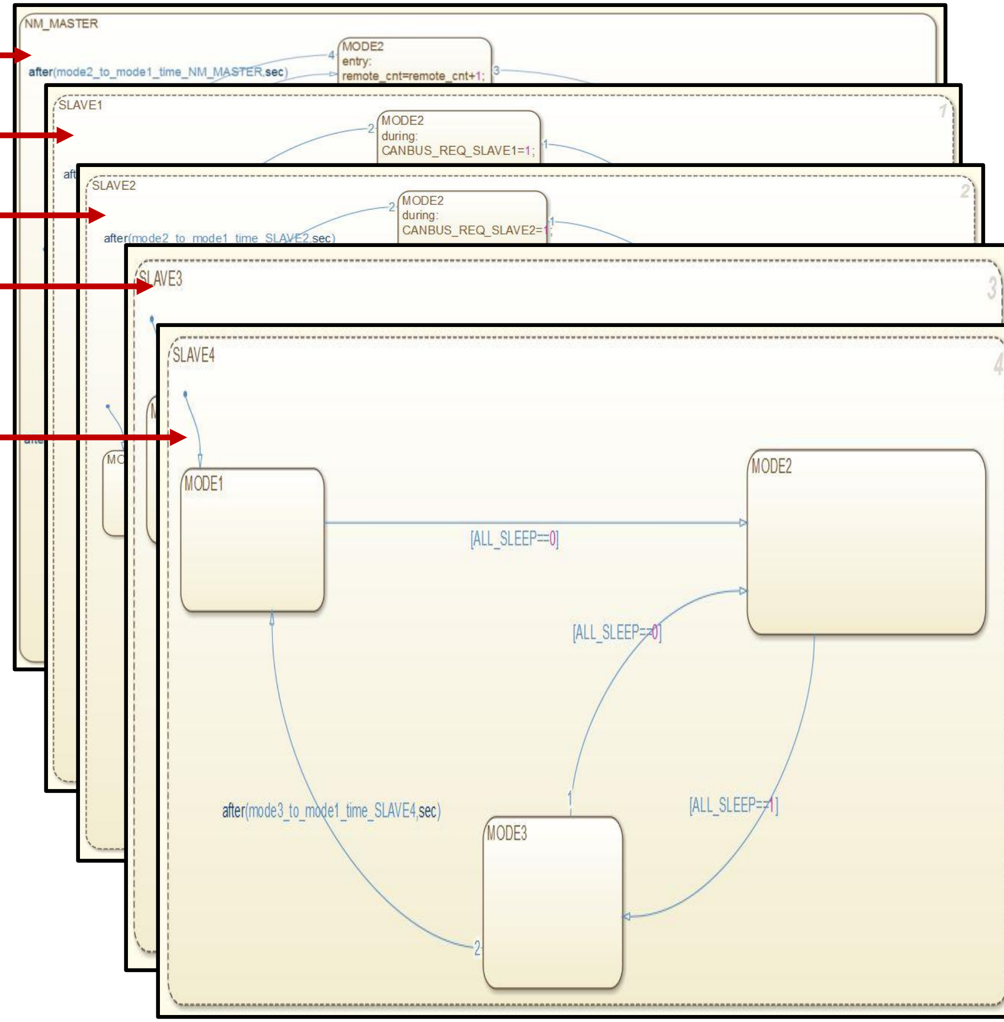
This document describes the CAN wakeup strategy in which certain nodes (here being ECUs) are required to be functionally active with communication after IGN OFF.

3 CAN Wakeup

There are two concepts involved for wakeup communication: NM_MASTER and SLAVE. NM_MASTER node is the one that initiates communication on the detection of pre-defined triggers. Based on these triggers the NM_MASTER node would initialize and send CAN messages on CAN port to other nodes in network. SLAVE node is the one which on receiving a wakeup message performs the activities intended.

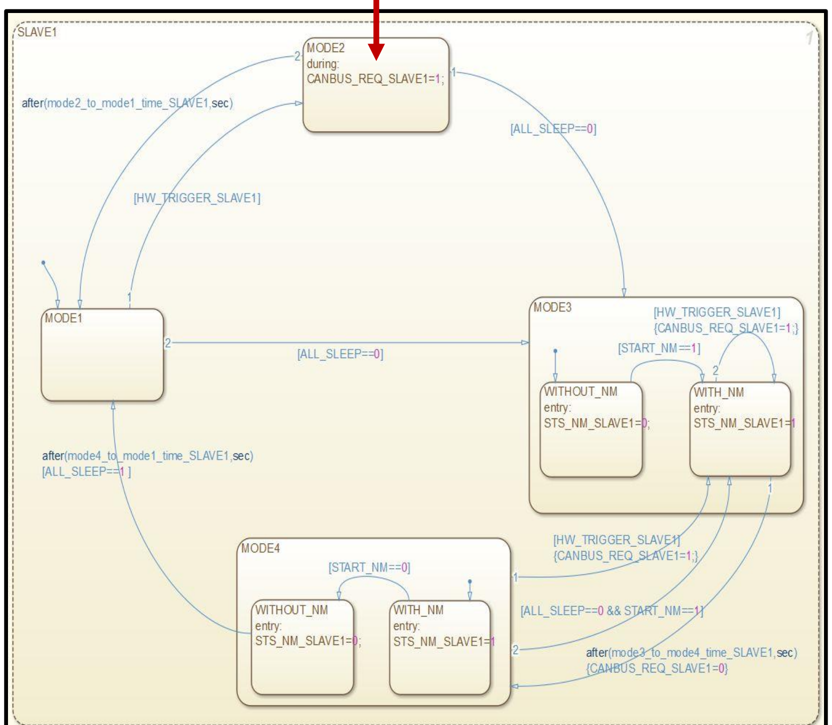
For proceeding with the logic to be implmented consider the following ECUs:

1. NM_MASTER
2. SLAVE1
3. SLAVE2
4. SLAVE3
5. SLAVE4

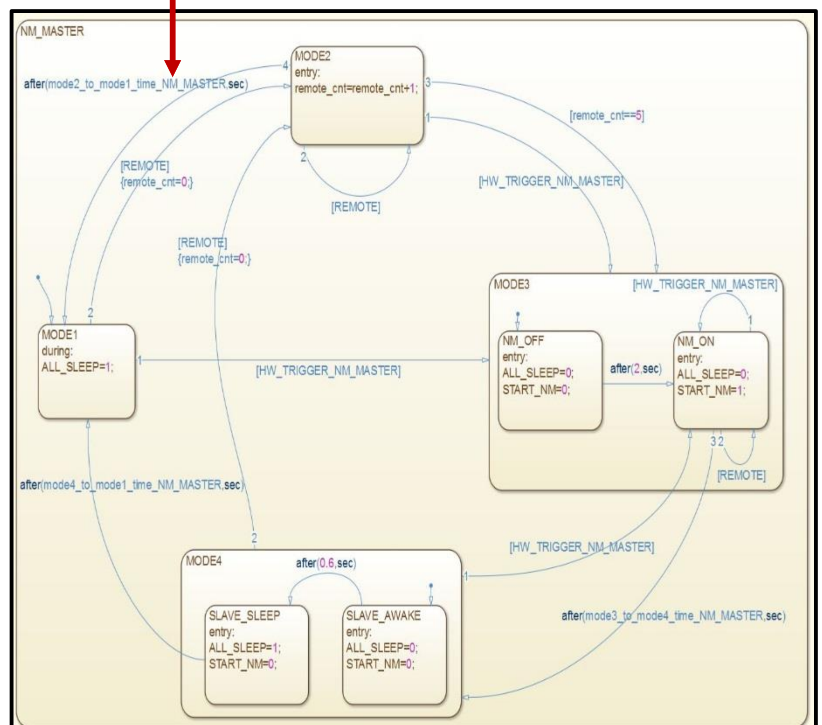


REQUIREMENT TRACEABILITY AND MODELLING

CANBUS_REQ_XXX: This signal would be tranmitted by any node that requires CAN Bus to be alive.



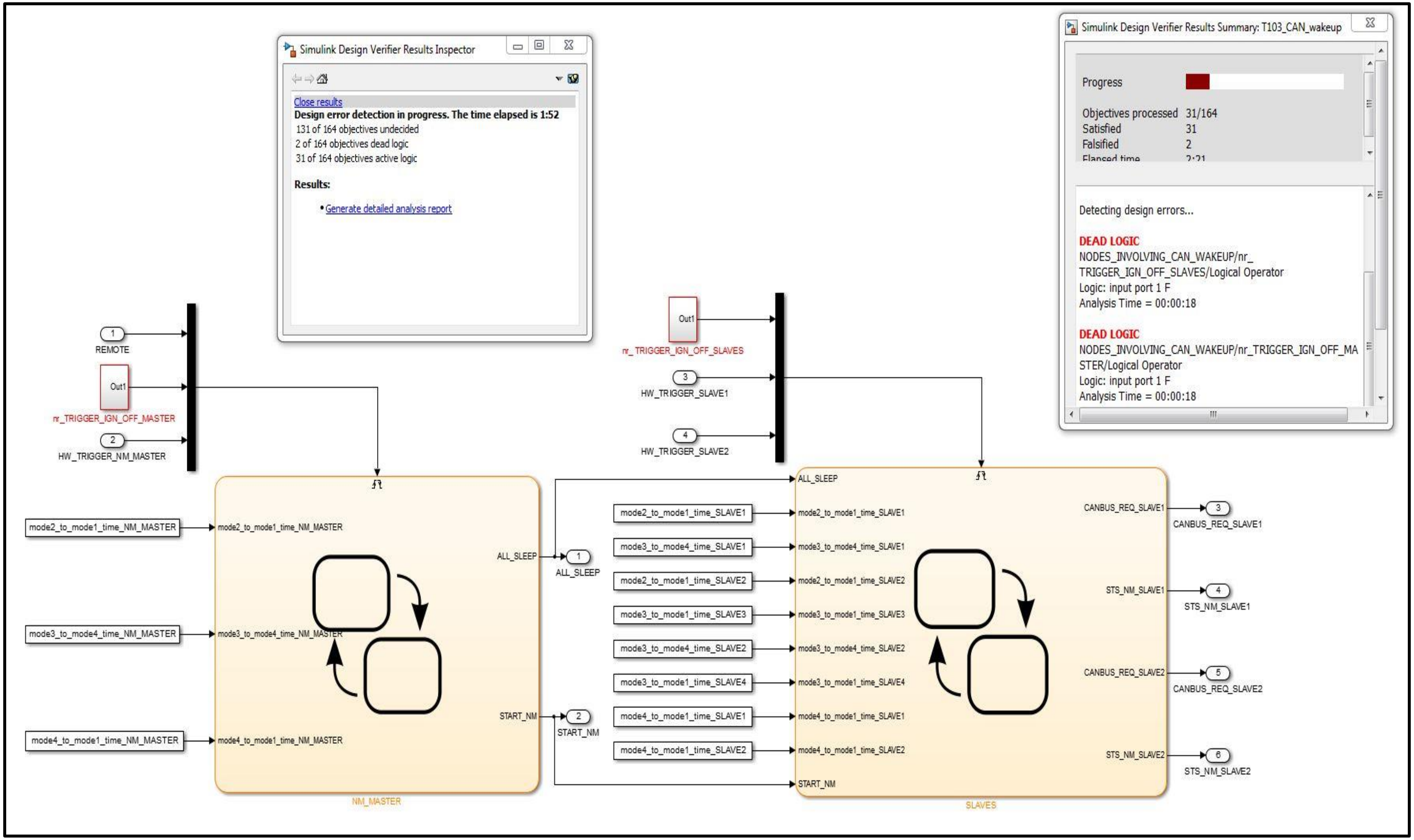
If the NM_MASTER gets less than 5 REMOTE triggers then after a calibratable time it should come back to MODE1.



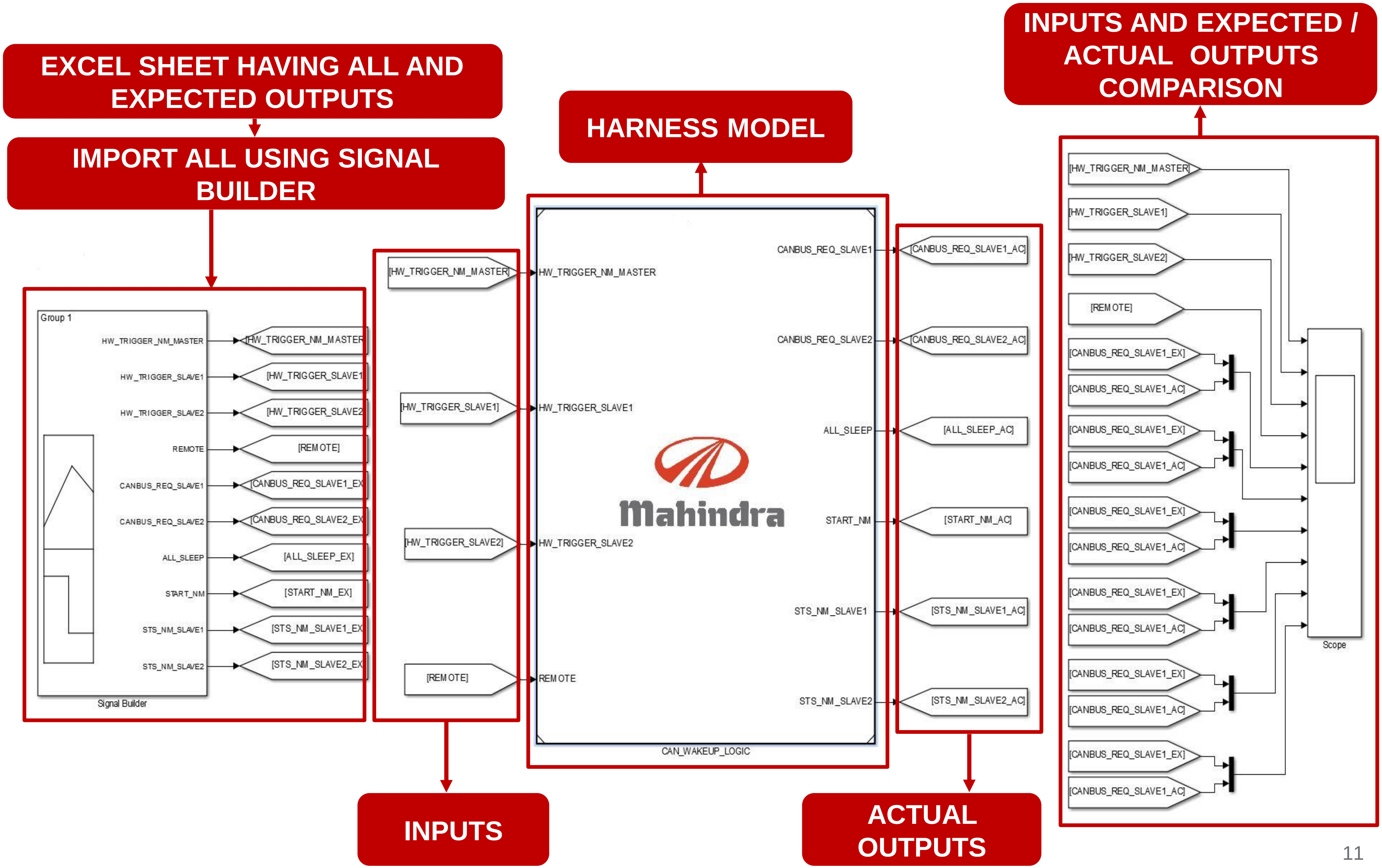
VALIDATION

- Design Error detection using Simulink Design Verifier
- Test case generation and validation using excel sheet / signal builder
- Coverage analysis
- Creating Hardware-In-Loop environment for actual ECU testing

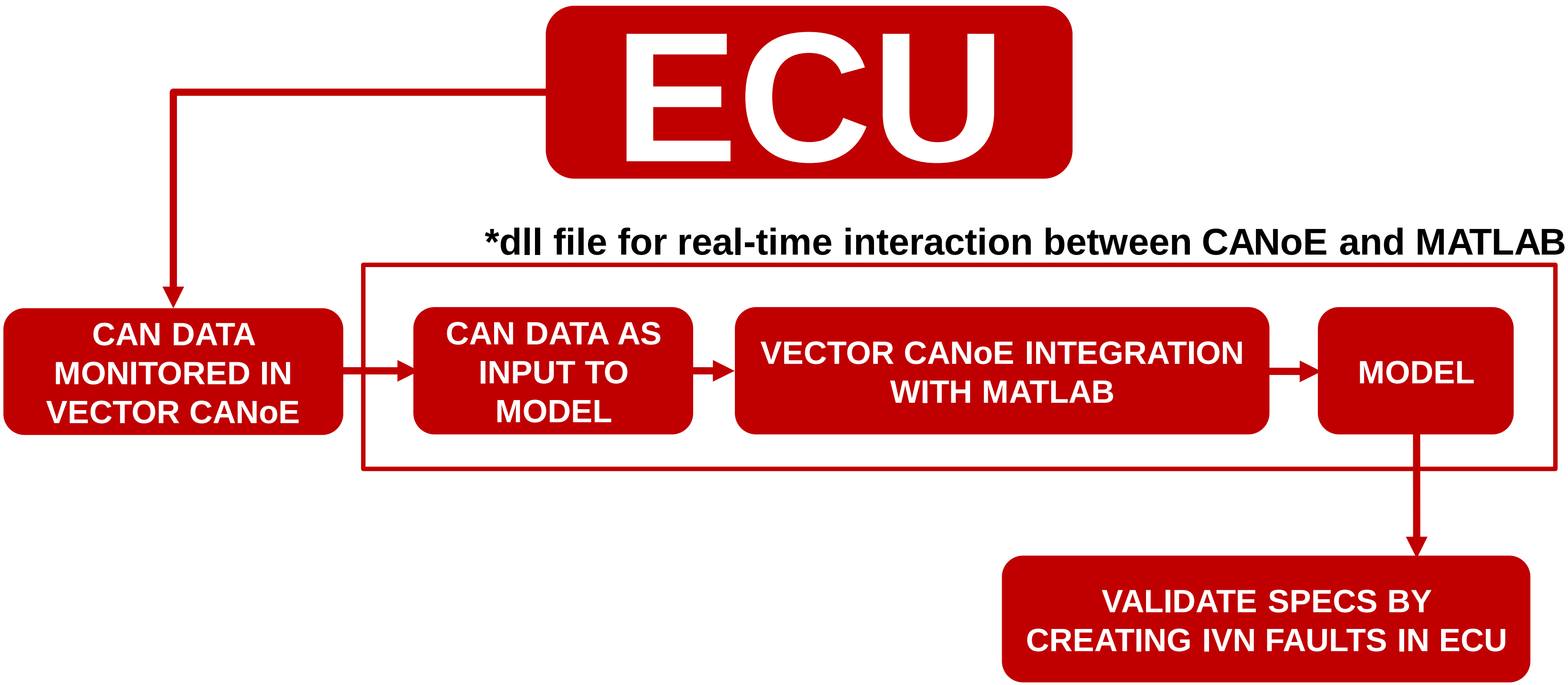
DESIGN ERROR DETECTION



SIGNAL BUILDER



HARDWARE-IN-LOOP



RESULTS

PROBLEM	TARGET ACHIEVED
Communication gap as most of our suppliers are from North-East Asia	→Visibility and readability of specs improved drastically →Real time simulation of specs
Huge development time	→ 40% reduction in development time and software deliveries
Delay in software deliveries	
Numerous software bugs	→ Iterations of buggy software reduced to 80%

TOOLS USED

- Simulink
- Stateflow
- Simulink Design Verifier
- Simulink Verification and Validation
- Vector CANoe Integration with MATLAB
- Report Generator

QUESTIONS

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THANK YOU

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